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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,999	05/12/2001	Rochit Rajsuman	ADTST.029AUS	6875

7590 11/15/2004

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EXAMINER
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BRITT, CYNTHIA-H

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 11/15/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/853,999

Applicant(s)

RAJSUMAN, ROCHIT

Examiner

Cynthia Britt

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,4 and 6-8 is/are rejected.
- 7) ☒ Claim(s) 2,5 and 9 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

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### **DETAILED ACTION**

Claims 1-9 are presented for examination.

#### ***Claim Objections***

Claims 2, 5 and 9, are objected to because of the following informalities:  
In line 5 of claim 2 and 5, and in lines 3 and 4 of claim 9, "...accessible of the internal..." is unclear. Appropriate correction is required.

#### ***Allowable Subject Matter***

Claims 2, 5 and 9, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and also the grammatical corrections indicated in the above objection.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 4, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. U. S. Patent No. 6,218,726 in view of Moberly U.S. Patent No. 6,484,280.

As per claims 1, 4, and 8, Chang et al teach An IC die formed with built-in stress test pattern and a method for forming such pattern are described. The stress test pattern may be formed by first forming a thermal oxide insulation layer on a silicon substrate, then forming a first plurality of diagonally positioned linear metal traces of a first metal, then depositing an electrically insulating material layer on top of the first plurality of diagonally positioned metal traces, and forming a second plurality of L-shaped metal bars of a second metal positioned with the two sides of L parallel to the two sides of a corner region and overlapping the first plurality of metal traces with the electrically insulating material layer therein between. The double metal method for forming the stress test pattern can be easily incorporated into the fabrication process for an IC die without any additional deposition or photolithographic steps. The metal 1 and metal 2 layers may be suitably formed of aluminum or an aluminum alloy, or any other conductive metallic material. (Column 3 lines 4-13) Not explicitly disclosed is that the system being tested is a SOC (System on a chip).

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However, in an analogous art, Moberly teaches a SOC design that is decomposed into functional blocks and surrounded by scan path cells. The simulation model of a chosen functional block is loaded into a field programmable gate array (FPGA) or similar device. A test pattern is applied to the chosen functional block using the scan path cells, and is also applied to the FPGA simulation of the chosen block. After toggling the clock, the results are read out and compared. If the result vectors from the chosen functional block and its FPGA simulation fail to match, a record is created for further analysis. The FPGA may be rapidly reconfigured to test other blocks of the SOC device. The FPGA may also be used to provide appropriate signal levels on other pins of the SOC device. (Column 2, lines 7-23) Therefore, it would have been obvious to a person having ordinary skill in the art at the time of this invention to have used the method of Chang et al. using the formation of the test pads to perform a built in stress test with the method of Moberly of functional testing a SOC. This would have been obvious to a person having ordinary skill in the art at the time this invention was made as suggested by Moberly (column 1 lines 15-18) in order to increase the accessibility of internal functional elements for testing.

As per claims 3, 6, and 7, Chang et al. teach the built-in stress test pattern formed on IC dies can be used to evaluate the various processing conditions and materials utilized in forming the dies. In the stress test pattern, each of the L-shaped metal bars and each of the metal traces are electrically connected to a contact pad adapted for contact probing such that a current flowing between the metal bar and the metal trace can be determined. The stress test pattern is

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formed by a double metal approach of utilizing a metal 1 and a metal 2 layer insulated between by an isolation layer for predicting thermo-mechanical stresses between the various material layers in the device. The metal 1 and metal 2 layer are deposited by normal fabrication processes utilized in forming the IC device and therefore, no additional masking or photolithographic process is required. The metal layers are first deposited by a typical metal deposition step, and then etched to form the specific patterns. For instance, for the metal 1 layer, an aluminum layer or an aluminum alloy layer is first deposited and then etched into diagonally positioned linear metal traces at a corner region of the IC die. Similarly, the metal 2 layer may be deposited of a conductive metal and then etched into L-shaped metal bars on top of an isolating layer deposited between the metal 1 layer and the metal 2 layer. (Column 4 lines 41-67)

### ***Conclusion***

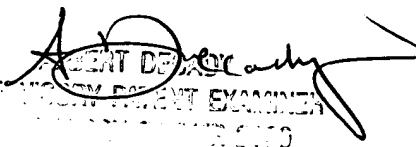
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Cynthia Britt  
Examiner  
Art Unit 2133

  
AGENT DEPOSE  
CYNTHIA BRITT EXAMINER  
ART UNIT 2133